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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/660,753	09/13/2000	Chin-Huang Chang	6319-56134	7237

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Klarquist Sparkman Campbell
Leigh & Whinston LLP
One World Trade Center Suite 1600
121 S W Salmon Street
Portland, OR 97204

EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	11

DATE MAILED: 12/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/660,753	Applicant(s) CHANG, CHIN-HUANG YB
	Examiner Lan Vinh	Art Unit 1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,11,19 and 20* is/are rejected.

7)☒ Claim(s) *9 and 12-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 11/12/2002 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/660753 is acceptable and a RCE has been established. An action on the RCE follows.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 11, 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 6 of claim 1 and line 9 of claim 11, the claim language of "to reduce semiconductor unit volume" is vague and indefinite because the term " semiconductor unit volume" has not been defined in the specification or in the claims. The examiner suggests replacing "to reduce semiconductor unit volume" with --to reduce semiconductor unit thickness--

In line 7 of claim 19, the claim language of "to reduce die volume" is vague and indefinite because the term " die volume" has not been defined in the specification or in the claims. The examiner suggests replacing "to reduce die volume" with --to reduce die thickness--

4. For the purpose of examination, the term "semiconductor unit" is defined as a "flip chip " in page 4 of the specification, the term "the size of the semiconductor unit meets an expected specification" is defined as the semiconductor unit reaches a specified thickness ranging from 2 mil to 6 mil in pages 3 and 4 of the specification. The term "to reduce semiconductor unit volume" and "to reduce die volume", as best understood by the examiner, as to reduce the thickness of the semiconductor unit and the thickness of the die.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goruganthu et al (US 6,069,366) in view of Hudak et al (US 5,656,552)

Goruganthu discloses a method of endpoint detection for thinning of silicon of a flip chip (claimed semiconductor unit) to make a bonded integrated circuit/package that includes a carrier 130 and flip chip die 100/semiconductor unit, the flip chip 100 includes a circuit side110/first surface and a back side 120/second surface, the second surface having no electrical connection device thereon (fig. 1). This method comprises the steps of:

attaching the circuit side 110/first surface to the pad 130/carrier (col 5, lines 36-38; fig. 1) which reads on attaching at least a part of the first surface to the carrier

etching the back side/second surface 120 of flip chip die100 to reduce the thickness of the die (col 5, lines 50-59; fig. 2) which reads on etching the semiconductor unit from the second surface to reduce semiconductor unit volume

Unlike the instant claimed invention as per claim 1, Goruganthu does not specifically discloses etching the semiconductor unit from the second surface to reduce semiconductor unit volume until the size of the semiconductor unit meets an expected specification/ the semiconductor unit reaches a thickness ranging from 2 mil to 6 mil

However, Hudak discloses a method for making thin conformal IC (integrated circuit) chip module comprises the step of etching the bottom surface of the die to thin down/ reduce the thickness of the IC die to 50 microns or approximately 2 mils (25.4 microns equal 1 mil) (see prior art of record for evidence of this basis) (col 8, lines 20-22). Husak's etching step reads on etching the surface of the IC die/semiconductor unit until the size of the semiconductor unit meets an expected specification/ the semiconductor unit reaches a specified thickness ranging from 2 mil to 6 mil

Since both Goruganthu and Hudak are concerned with method of etching to reduce the thickness of a IC die, one skilled in the art would have found it obvious to modify Goruganthu's etching step by etching the surface of the IC die/semiconductor unit until the size of the semiconductor unit meets an expected specification as per Hudak since Hudak teaches that by thinning the IC die to a thickness less than or equal to 50

microns / 2mil, a planarization step required by prior art method may be eliminated (col 4, lines 65-67)

Regarding claim 2, Goruganthu discloses etching by a laser beam/beam of light (col 5, lines 56-58)

Regarding claim 3, Goruganthu discloses etching using gas to remove silicon from die/to reduce the thickness of the die (col 6, lines 1-8)

The limitation that the expected specification means that the thickness of the semiconductor unit measured relative to the first surface is within a specified range, as recited in claim 4, has been discussed above

Regarding claim 5, Goruganthu discloses that the die 100/semiconductor unit is attached to the pad/carrier 130 by solder bumps (col 5, lines 27-29) which reads on the die 100/semiconductor unit is attached to the carrier by bumps configuration

Regarding claim 10, since Goruganthu discloses using surface 130 as a package for a flip chip die 100 (col 5, lines 28-30) and fig. 1 of Goruganthu shows that package 130 carries flip chip die 100, Goruganthu's surface 130 reads on a chip carrier. Goruganthu also discloses that the die 100 includes solder bumps/electrical connection device located on the circuit side110/first surface, the solder bumps connect the die 100 and surface 130/chip carrier (col 5, lines 27-29; fig. 2)

7. Claims 6, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goruganthu et al (US 6,069,366) in view of Hudak et al (US 5,656,552) and further in view of Bruce et al (US 6,417,068)

Goruganthu as modified by Hudak has been described above in paragraph 6. Unlike the instant claimed inventions as per claims 6, 8, Goruganthu and Hudak fail to disclose using a fixture to shield at least part of semiconductor unit and the carrier to prevent the etching from affecting the quality of the semiconductor unit and the carrier.

However, Bruce discloses a method for milling the substrate of a semiconductor device (flip chip die) comprises the step of using a fixture 28 to shield at least part of semiconductor unit and the carrier to prevent the etching from affecting the quality of the semiconductor unit and the carrier (col 5, lines 40-42; fig. 5 shows that fixture 28 shields/covers at least part of semiconductor unit 20 and the carrier 14 during laser beam etching to prevent the etching from affecting the quality of the semiconductor unit and the carrier

Since both Goruganthu and Bruce are concerned with method of etching a die using laser beam etching, one skilled in the art would have found it obvious to modify Goruganthu and Hudak by using a fixture 28 to shield at least part of semiconductor unit and the carrier as per Bruce because Bruce states that underfill material 28/fixture encapsulates the solder bumps connections and provide additional mechanical benefits (col 5, lines 41-43)

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Goruganthu et al (US 6,069,366) in view of Hudak et al (US 5,656,552) and further in view of Siniaguine (US 6,184,060)

Goruganthu as modified by Hudak has been described above in paragraph 6. Unlike the instant claimed inventions as per claim 7, Goruganthu and Hudak do not specifically disclose the step of grinding the IC die/semiconductor unit to a expected specification/ a specified thickness range before joining the IC die to the carrier although Goruganthu does disclose using a grinding device to thin the die (col 5, lines 40-42).

However, Siniaguine discloses a method for fabricating semiconductor die comprises the step of grinding the semiconductor wafer/unit to reduce the thickness of the semiconductor wafer/unit to a specified thickness before dicing the wafer into chip (col 8, lines 48-50)

Since Goruganthu discloses using a grinding device to thin the die, one skilled in the art would have found it obvious to modify Goruganthu and Hudak grinding step by grinding the die/semiconductor unit to reduce the thickness to a specified thickness as taught by Siniaguine since Siniaguine states that it is known that silicon is removed from the semiconductor wafer/semiconductor unit by mechanical grinding to reduce the wafer thickness to a specified range (col 8, lines 47-50)

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine (US 6,184,060) in view of Goruganthu et al (US 6,069,366)

Siniaguine discloses a method for fabricating semiconductor die/semiconductor unit, the die having a face side/first surface and a back side/second surface, the face side/first surface has circuitry/electrical connection formed thereupon (col 8, lines 45-47; fig. 17C) . This method comprises the steps of:

dicing the wafer into a plurality of chips/dices (col 8, lines 50-51)

placing/moving the chip/die into the chip holder 1610 /seating apparatus to expose the back side/second surface of the die (col 8, lines 56-58; fig. 18)

applying plasma on the back side/second surface of the chip/die to thin/reduce the thickness of the exposed second surface of the chip/die (col 8, lines 52-54), fig. 18 shows that the chip holder 1610/seating apparatus shielding the face/first surface of the chip/die from being etched /immunizing one surface of the chip/die against the plasma

Siniaguine differs from the instant claimed invention as per claim 19 by applying plasma on the die surface to reduce the die thickness/die volume instead of applying beam of light to to reduce the die thickness

However, Goruganthu, in a method for thinning of semiconductor die, teaches that laser beam and reactive ion etching/plasma etching are known methods for removing silicon from semiconductor die to reduce the die thickness (col 5, lines 54-58; col 6, lines 1-12)

Hence, one skilled in the art would have found it obvious to substitute Siniaguine's step of applying plasma to reduce die thickness with applying laser beam to reduce the die thickness in view of Goruganthu's teaching because both plasma etching and laser beam etching are known method for reducing the semiconductor die thickness, thus the substitution of one for the other would have produced an expected result.

10. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine (US 6,184,060) in view of Goruganthu et al (US 6,069,366) and further in view of Hudak et al (US 5,656,552)

Siniaguine as modified by Goruganthu has been described above in paragraph 9. Regarding claim 20, Siniaguine discloses the step of moving the die from the chip holder 1610/seating apparatus to encapsulate/attach the die to a ceramic package/chip carrier by contact pads/electrical connection on the back side/second surface of the die (col 6, lines 38-40, col 9, lines 1-2). Unlike the instant claimed invention as per claim 20, Siniaguine and Goruganthu do not specifically discloses ending/stopping the etching step when the size (thickness) of chip/die meets an expected specification/a specified range of thickness between 2 mil-6mil.

However, Hudak discloses a method for making thin conformal IC chip module comprises the step of using RIE etching/plasma etching to thin down the thickness of the IC chip/die to 50 microns or approximately 2 mil (25.4 microns equal 1 mil) (see prior art of record for evidence of this basis) (col 8, lines 20-22). Husak's etching step reads on stopping the etching when the size (thickness) of the IC chip meets an expected specification/a specified range of thickness between 2 mil-6mil.

Since both Siniaguine and Hudak are concerned with method using plasma etching to reduce the thickness of a IC chip, one skilled in the art at the time the invention was made would have found it obvious to modify Siniaguine and Goruganthu by stopping the etching when the size (thickness) of the semiconductor unit meets an expected specification/a specified range as per Hudak especially since Hudak discloses that by

thinning the IC chip/die to a thickness less than or equal to 50 microns/ 2mil , a planarization step required by prior art method may be eliminated (col 4, lines 65-67)

Allowable Subject Matter

11. Claim 11 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claims 12-18 are objected to as being dependent upon a rejected claim, but would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 9, 11, the prior art of record fails to teach etching the semiconductor unit to reduce semiconductor unit thickness/volume wherein the semiconductor unit is attached to the carrier in a configuration of lead-on-chip. The closest prior art of Gorugathu et al (US 6,069,366) discloses etching the semiconductor unit to reduce semiconductor unit thickness/volume wherein the semiconductor unit is attached to the carrier in a configuration of flip-chip

Response to Arguments

12. Applicant's arguments with respect to claims 1-8, 10, 19, 20 have been considered but are moot in view of the new ground(s) of rejection.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Myer et al (US 4,872,945) discloses that 25.4 microns being equal to 1mil (col 5, lines 20-22)

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

LV
December 12, 2002